



INFORMATION CITED BY APPLICANTS THAT MAY BE MATERIAL TO THE
PROSECUTION OF THE SUBJECT APPLICATION

Applicants: T. Hironaka et al. Attorney Docket No.: SUSU121842
Application No.: 10/687,460 Art Unit: 2188 / Confirmation No.: 8870
Filed: October 15, 2003
Title: MULTI-PORT INTEGRATED CACHE

U.S. PATENT DOCUMENTS

*Examiner Cite Initials	No.	Document No.	Kind Code	Date (mm/dd/yyyy)	Name
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None

FOREIGN PATENT DOCUMENTS

*Examiner Cite Initial	No.	Document No.	Kind Code	Publication Date (mm/dd/yyyy)	Country	English Abstract Provided	Translation Provided
JS	F1	JP 4-257949	A	09/14/1992	JP		
JS	F2	JP 2002-55879	A	02/20/2002	JP		

OTHER INFORMATION

(Including Author, Title, Date, Pertinent Pages, Etc.)

*Examiner Initial	Cite No.	
JS	O5	Mattauch, H.J., "Hierarchical N-Port Memory Architecture Based on 1-Port Memory Cells," Research Center for Nanodevices and Systems, Hiroshima University, Higashi-Hiroshima, Japan, p. 348-352.

Examiner

/Jasmine Song/

Date Considered

10/30/2006

*Examiner: Initial if reference considered, whether or not citation is in conformance with M.P.E.P. § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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JS	O1	Mattausch, H.J., et al., "Area-Efficient Multi-Port SRAMs for On-Chip Data-Storage with High Random-Access Bandwidth," <i>IEICE Transactions on Electronics E84-C(3)</i> :410-417, 2001.
JS	O2	Mattausch, H.J., and K. Yamada, "Application of Port-Access-Rejection Probability Theory for Integrated N-Port Memory Architecture Optimisation," <i>Electronics Letters 34(9)</i> :861-862, 1998.
JS	O3	Mattausch, H.J., "Hierarchical Architecture for Area-Efficient Integrated N-Port Memories with Latency-Free Multi-Gigabit Per Second Access Bandwidth," <i>Electronics Letters 35(17)</i> :1441-1443, 1999.
JS	O4	Tatsumi, Y., and H.J. Mattausch, "Fast Quadratic Increase of Multiport-Storage-Cell Area with Port Number," <i>Electronics Letters 35(25)</i> :2185-2187, 1999.

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